Amendments to the Specification:

Please replace paragraph 0047 with the following amended paragraph:

Various embodiments of the present invention provide numerous advantages, although it will be appreciated that only some embodiments may provide all the advantages while other embodiments provide fewer advantages. One advantage of an architecture includes the scalability of processing throughput as a function of the speed and number of processors. Dispatch logic, such as dispatch logic 106 and 107, assign packets to ~~specific~~ a specific processor. This allows each processor to run a separate thread of a TCP/IP network protocol stack. This eliminates most coherency and serialization normally seen in systems with multiple processors. An architecture of the invention also has the advantage that it supports future changes and enhancements to a network protocol stack such as the TCP/IP protocol stack. Since the network protocol stack processing is performed in software which is being executed by each processor, such as processor 102A, 102B, and 102N, and since the fields used to generate the hash function to assign packets to target processors is programmable, enhancements and changes to the TCP/IP suite of protocols can be supported via software changes. Another advantage of an architecture of the invention is an improvement in memory bandwidth. Memory bandwidth is one of the main bottlenecks in network processing, both when processing the network protocol stack in the primary processor (e.g. a Pentium microprocessor) of a general purpose computer or when offloaded to a network protocol processing device such as the accelerator 64 shown in **Figure 5**. Designating preallocated memory buffers for use by the dispatch and queue control logic within logic 106 and 107 allows the packets to be copied to their final memory location. Another advantage to an architecture of the present invention is the reduction of interrupts in the processing of network packets. Dedicated DMA engines and control queues in the logic 106 and 107,

which transfer packets to and from both the network (e.g. Ethernet) interface and the host interface, eliminate processor idle time during the DMA operations. That is, the processors such as processors 102A, 102B and 102N, may perform network protocol processing with packets while other packets are undergoing DMA operations to and from interfaces 104 and 109. Another advantage of an architecture of the present invention is that the efficiency of the host processor is increased, since the host processor does not execute the network protocol stack. Host processor cycles which were consumed by network protocol processing are now freed up for application data processing.

Applicants respectfully submit that the above amendment does not add any new matter to the original specification. The amendment merely corrects a typographical error.